What is claimed is:

1. A semiconductor device comprising:

an MOS capacitor that comprises,

a first-conductivity-type diffusion layer formed in a surface of a substrate,

a gate oxide film formed on said first-conductivity-type diffusion layer, and

a first polysilicon layer formed on said gate oxide film and doped with a dopant of the first conductivity type or a second conductivity type; and

a Poly-Poly capacitor that comprises,

said first polysilicon layer,

a first dielectric layer formed on said first polysilicon layer, and

a second polysilicon layer formed on said first dielectric layer and doped with a dopant of the first conductivity type or the second conductivity type,

said Poly-Poly capacitor being stacked on said MOS capacitor, and

said first-conductivity-type diffusion layer and said second polysilicon layer being electrically connected to a same first metal interconnection.

2. The semiconductor device according to claim 1, further comprising a PN-junction capacitor comprising said first-conductivity-type diffusion layer and a second-conductivity-type diffusion layer formed under said first-conductivity-type diffusion layer,

wherein said first polysilicon layer, doped with a dopant of the second conductivity type, is electrically connected to said second-conductivity-type diffusion layer.

3. The semiconductor device according to claim 1, further comprising an MIM capacitor comprising:

a second metal interconnection electrically connected to said first polysilicon layer;

a second dielectric layer formed on said second metal interconnection; and

a third metal interconnection formed on said second dielectric layer and electrically connected with said first metal interconnection.

4. The semiconductor device according to claim 1,

wherein a second-conductive-type diffusion layer is formed under said first-conductivity-type diffusion layer, and

said semiconductor device further comprises a trench isolation oxide film capacitor comprising:

a trench isolation oxide film isolating said first-conductivity-type diffusion layer and said second-conductivity-type diffusion layer into individual element regions; and

first-conductivity-type trench side-wall diffusion layers formed on both side walls of said trench isolation oxide film, a portion of said first-conductivity-type trench side-wall diffusion layers being connected with said first-conductivity-type diffusion layer,

and wherein second metal interconnection electrically connects said first polysilicon layer and a portion of said first-conductivity-type diffusion layer that is in an element region adjacent to the element region where said MOS capacitor resides, with said trench isolation oxide film interposed therebetween.

5. A semiconductor device comprising:

a first Poly-Poly capacitor that comprises,

a spiral-shaped first polysilicon electrode,

a spiral-shaped second polysilicon electrode formed parallel to the shape of said first polysilicon electrode, and

a third dielectric layer interposed between said first polysilicon electrode and said second polysilicon electrode.

6. The semiconductor device according to claim 5, wherein said third dielectric layer has a higher dielectric constant than an interlayer insulating film formed on the semiconductor substrate.

7. The semiconductor device according to claim 5, further comprising a second Poly-Poly capacitor that comprises:

a spiral-shaped third polysilicon electrode;

a spiral-shaped fourth polysilicon electrode formed parallel to the shape of said third polysilicon electrode; and

a fourth dielectric layer interposed between said third polysilicon electrode and said fourth polysilicon electrode,

wherein said second Poly-Poly capacitor is disposed over said first Poly-Poly capacitor with a fifth dielectric layer interposed therebetween, with said fourth polysilicon electrode located above said first polysilicon electrode and said third polysilicon electrode located above said second polysilicon electrode, and

said first polysilicon electrode and said third polysilicon electrode are electrically connected to each other, and said second polysilicon electrode and said fourth

polysilicon electrode are electrically connected to each other.

8. The semiconductor device according to claim 7, wherein said first polysilicon electrode and said third polysilicon electrode are directly connected to each other, and said second polysilicon electrode and said fourth polysilicon electrode are directly connected to each other.

9. The semiconductor device according to claim 7, wherein said third dielectric layer, said fourth dielectric layer, and said fifth dielectric layer have a higher dielectric constant than an interlayer insulating layer formed on the semiconductor substrate.

10. The semiconductor device according to claim 7, further comprising an MOS capacitor that comprises:

said first polysilicon electrode and said second polysilicon electrode;

a gate oxide film formed under said first polysilicon electrode and said second polysilicon electrode; and

a diffusion layer formed under said gate oxide film and having a first conductivity type or a second conductivity type,

wherein said fourth polysilicon electrode and said diffusion layer are electrically connected to a same metal interconnection.